ISE Using Description

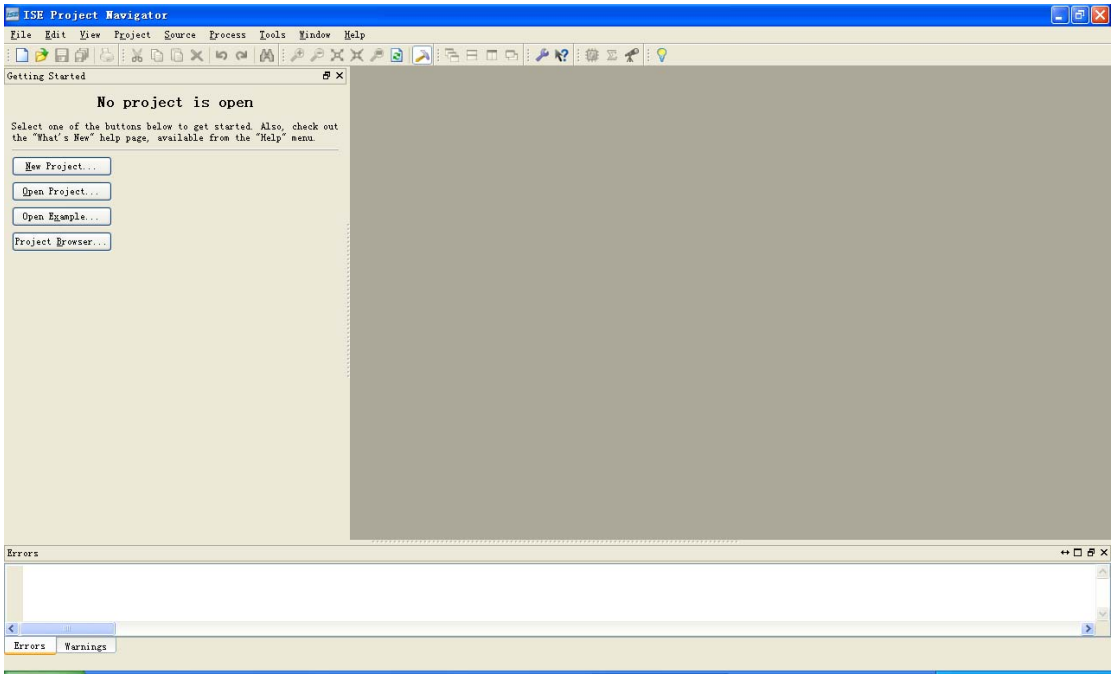
——Example led Experiment

Eleckits Studio

www.eleckits.com

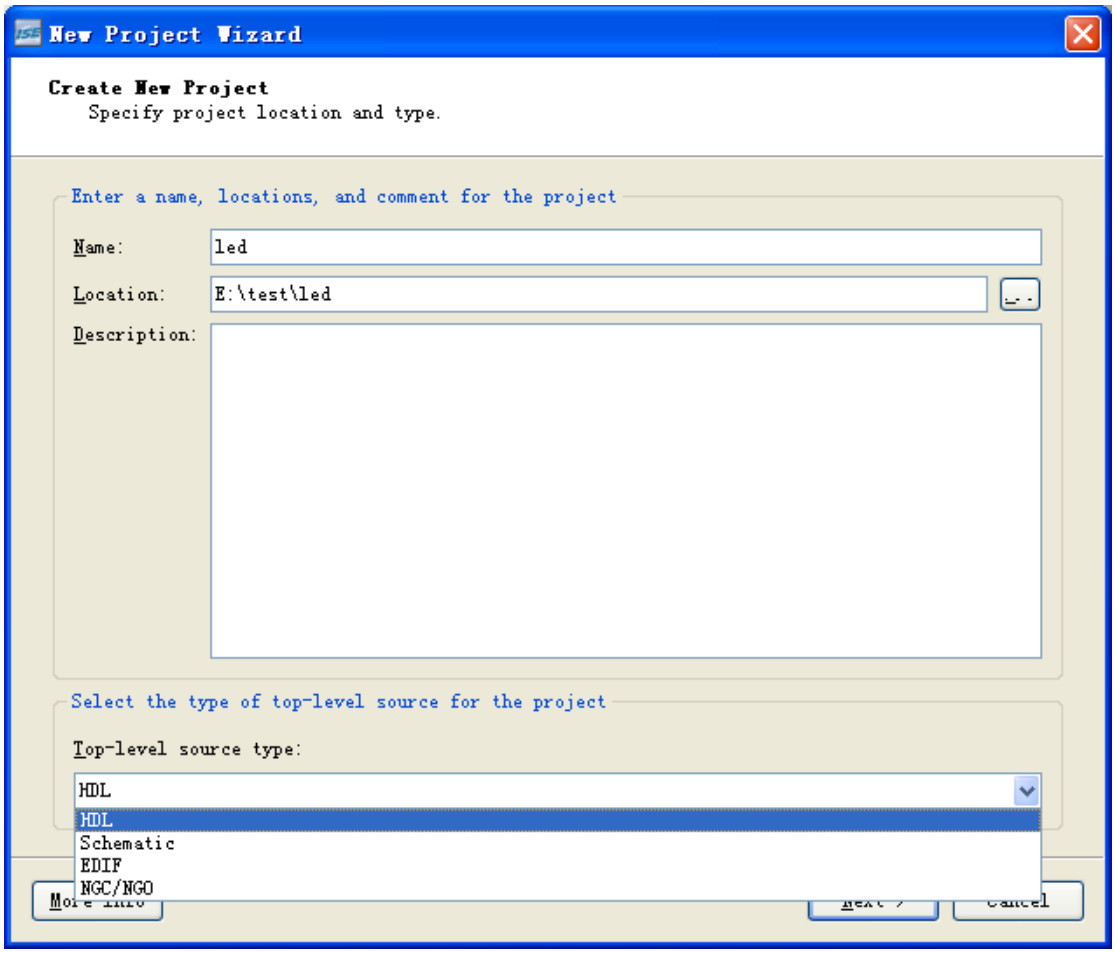
I、Start Xinlix ISE：

Click：start ⟶ all programs ⟶ Xilinx ISE 11 ⟶ Project Navigator

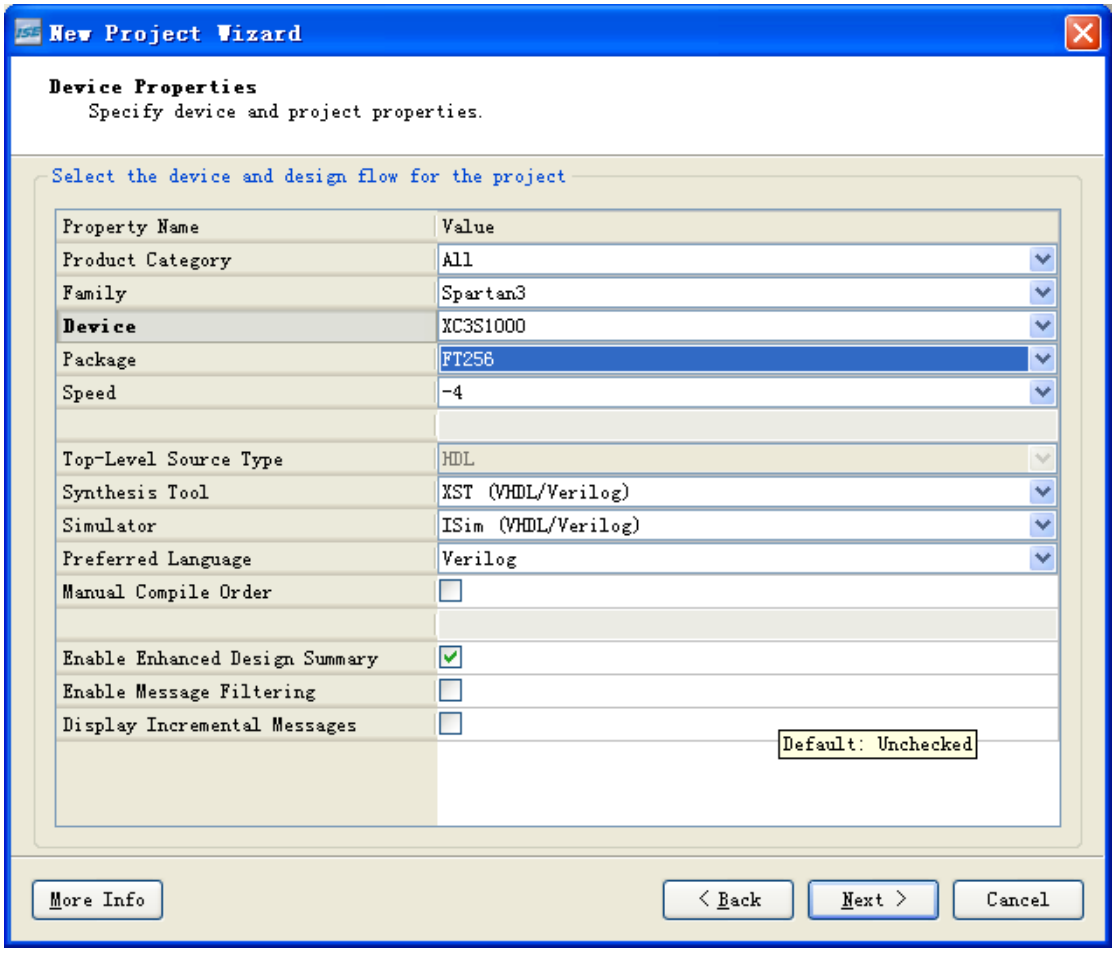


II、set up\open a project

If there is a project, in the pop dialog from File ⟶ Open Project choose your project. If there is no suitable project, you need to set up a new one through File New Project. Detailed steps are as following:



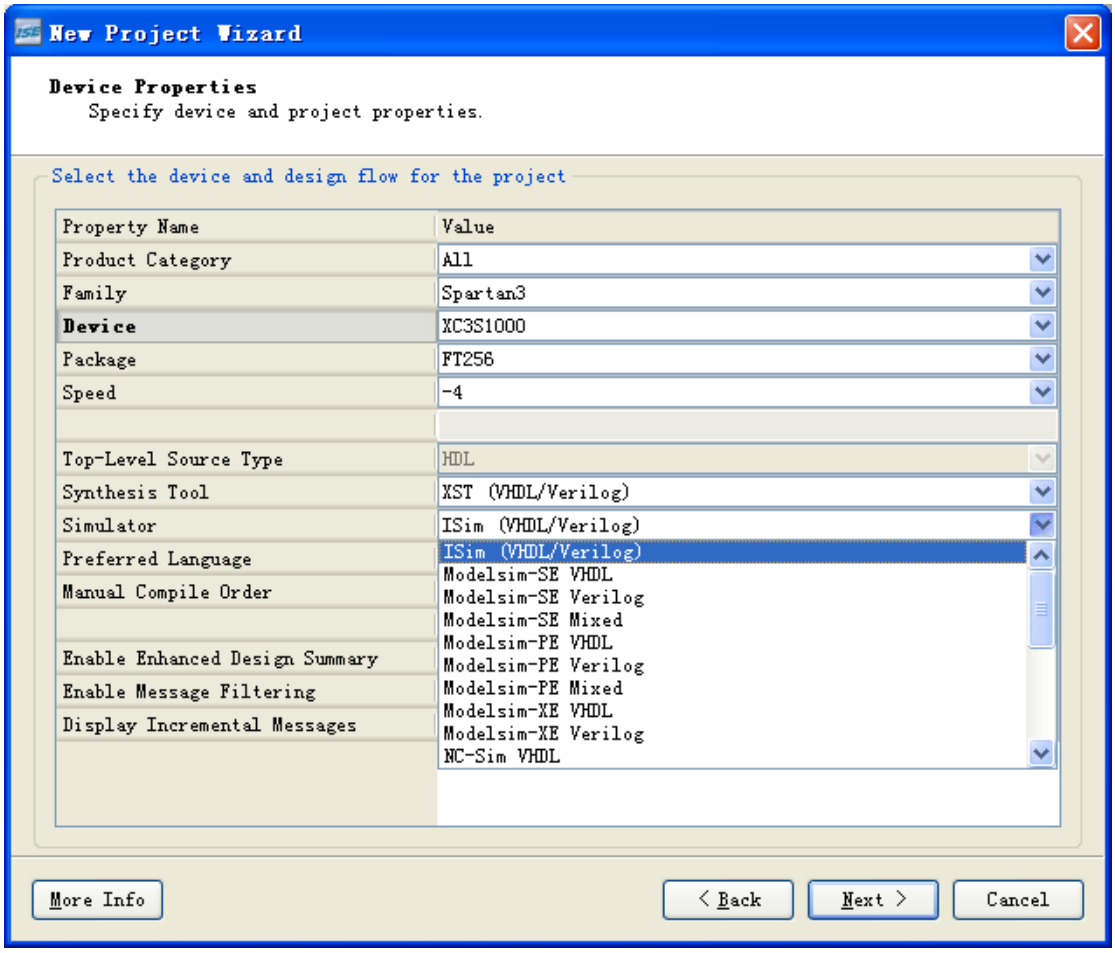
Fill the project name and path of the one you want to set up in Project Name and Project Location separately. In the drop-down menu of Top-level Module Type choose the top module type of your project. This LED experiment chooses HDL. Click Next:



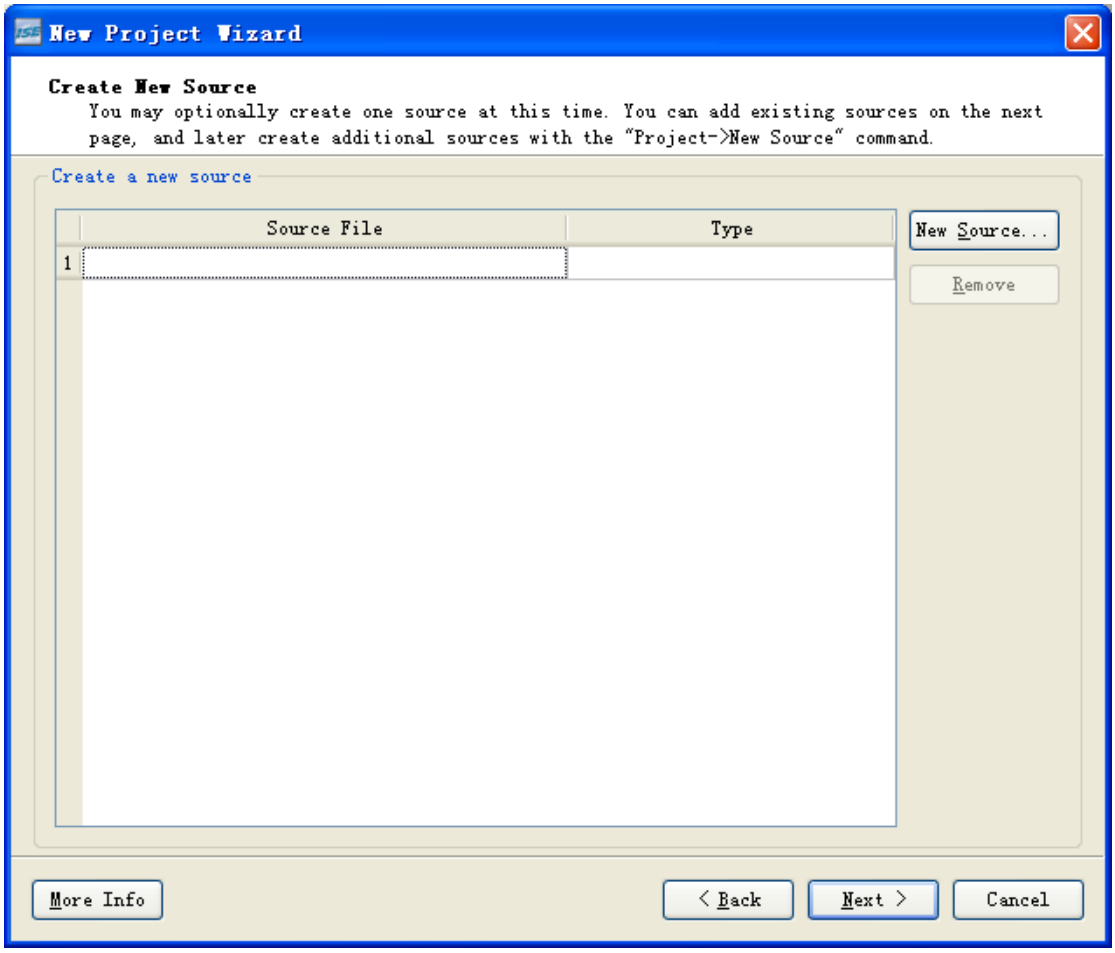
In this dialog choose:

Device Family	Used FPGA type
Device	Used FPGA model
Package	Used FPGA package
Speed Grade	Used FPGA speed
Top-Level Module Type	Top level module type
Synthesis Tool	Synthesis tool
Simulator	Simulator tool
Generated Simulation Language	Simulator module language type

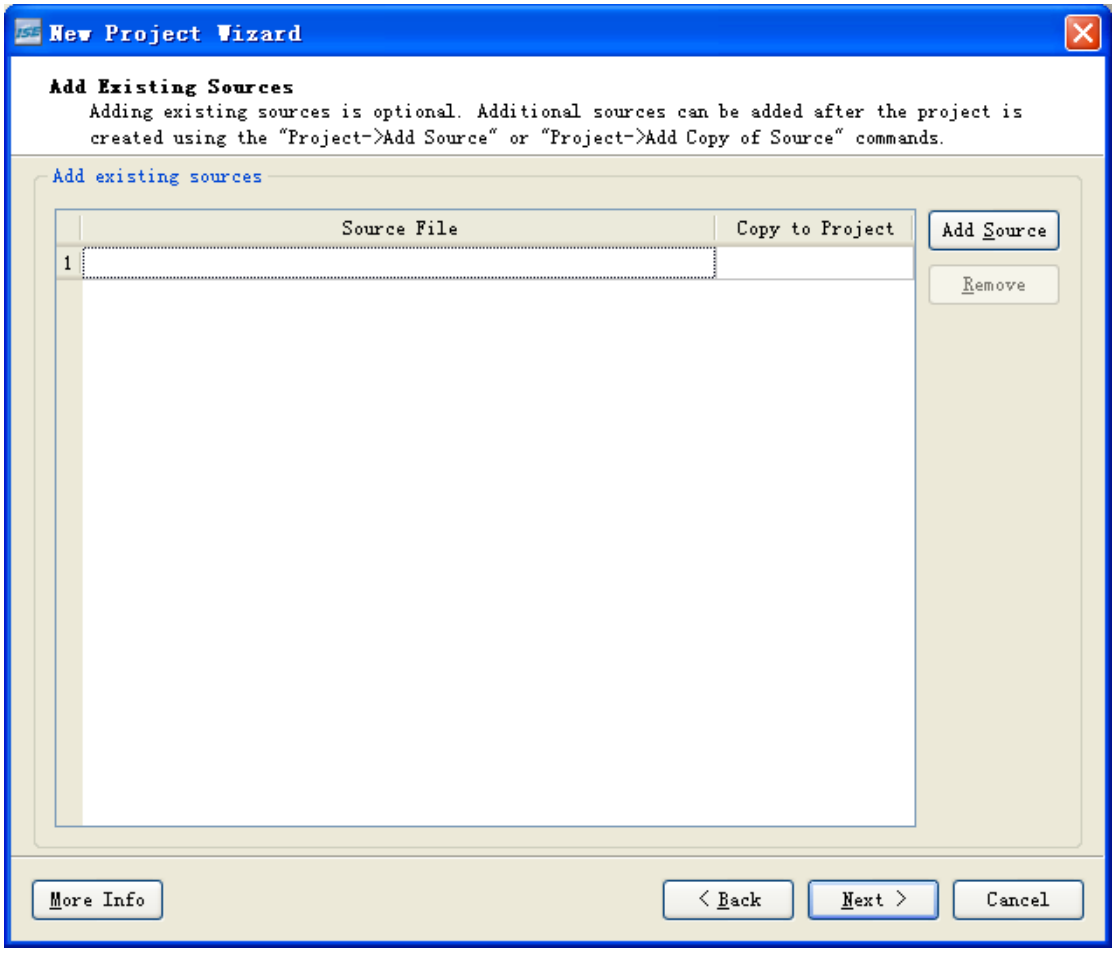
This experiment chooses synthesis tool and simulator tool ISE provided. Here you can also choose the third party's application software:



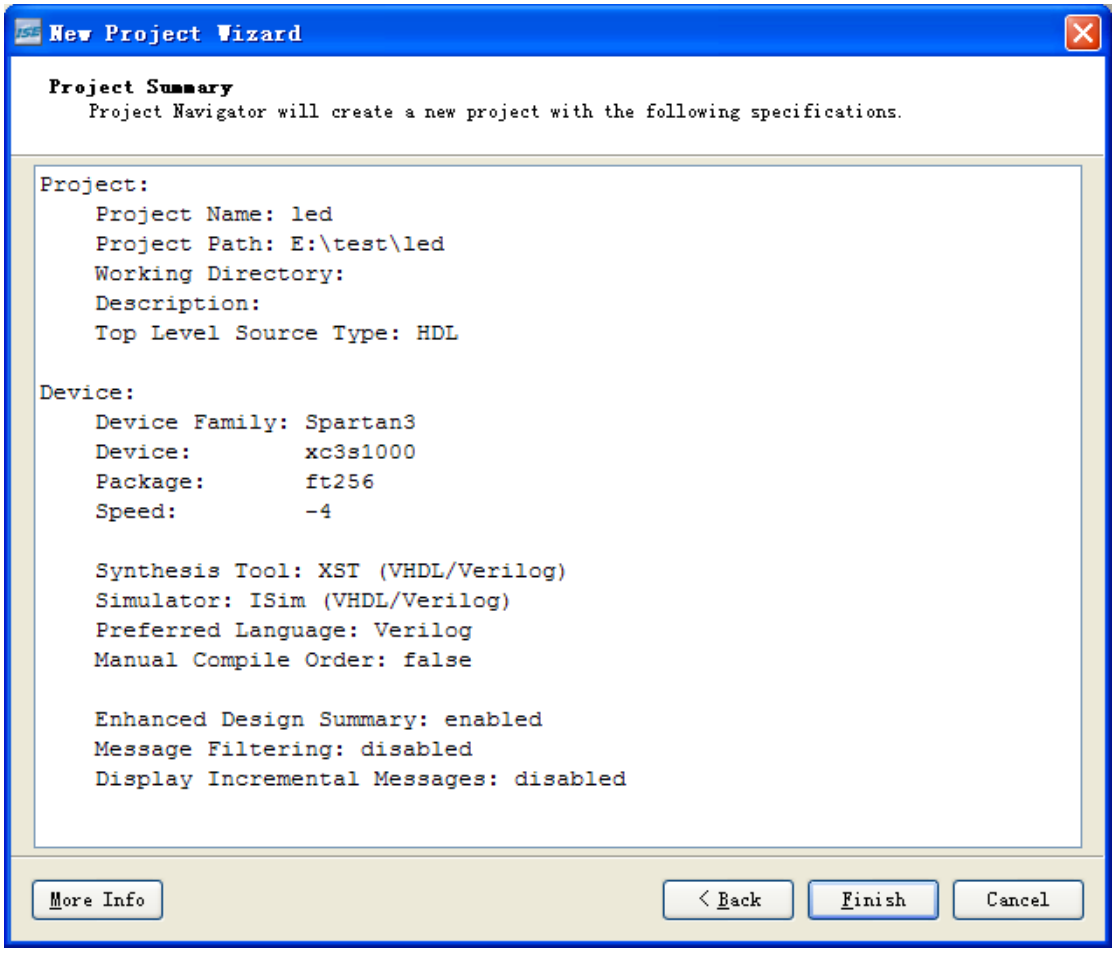
Modelsim and Synplify Pro are general third party simulator and synthesis software. Here if we choose third part software to simulator and synthesis, the ISE Navigator will search and open related software in the following steps. Fill FPGA type and used synthesis, simulator software and then, click Next:



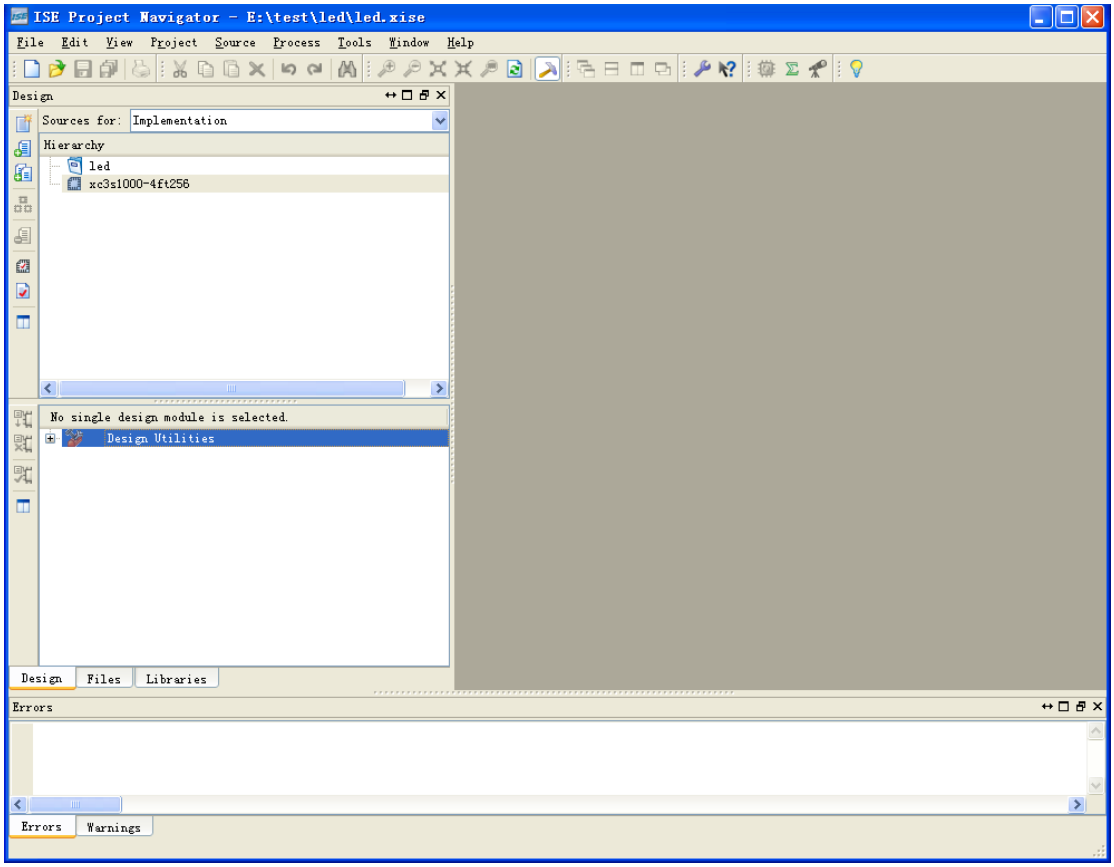
In this dialog, allow user to set up a new source file for the project to be set. Here can only set up one source file. Others have to be found after the project set. Or you may set up all source files after the project set. Here directly click Next:



In this dialog, add the existed source file for the project to be set up. If there is no existed source file, directly click Next:

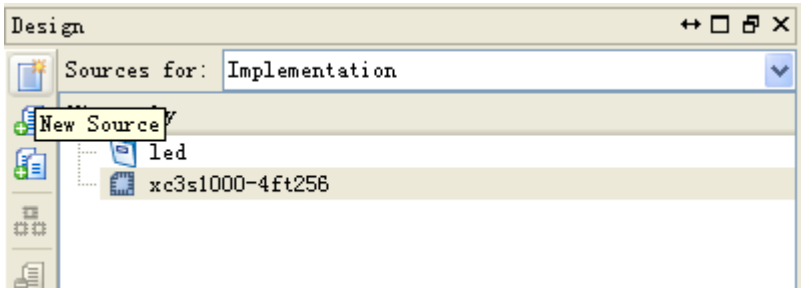


In this dialog, shows all of the information of the project to be set up. Confirm it and click finish. Project Navigator will set up one project named led automatically.

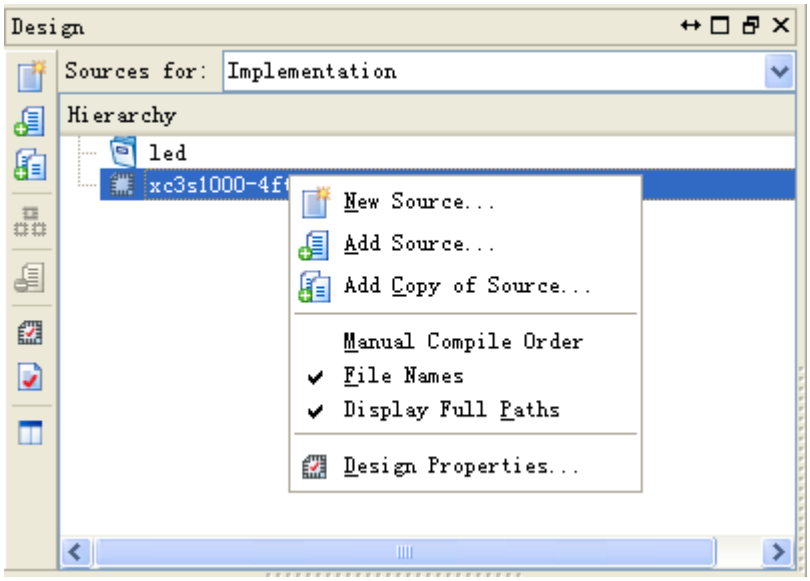

ISE Project Navigator - E:\test\led\led.xise
File Edit View Project Source Process Tools Window Help
Design
Sources for: Implementation
Hierarchy
led
xc3s1000-4ft256
No single design module is selected.
Design Utilities
Design Files Libraries
Errors
Errors Warnings

III. Add source files for the project

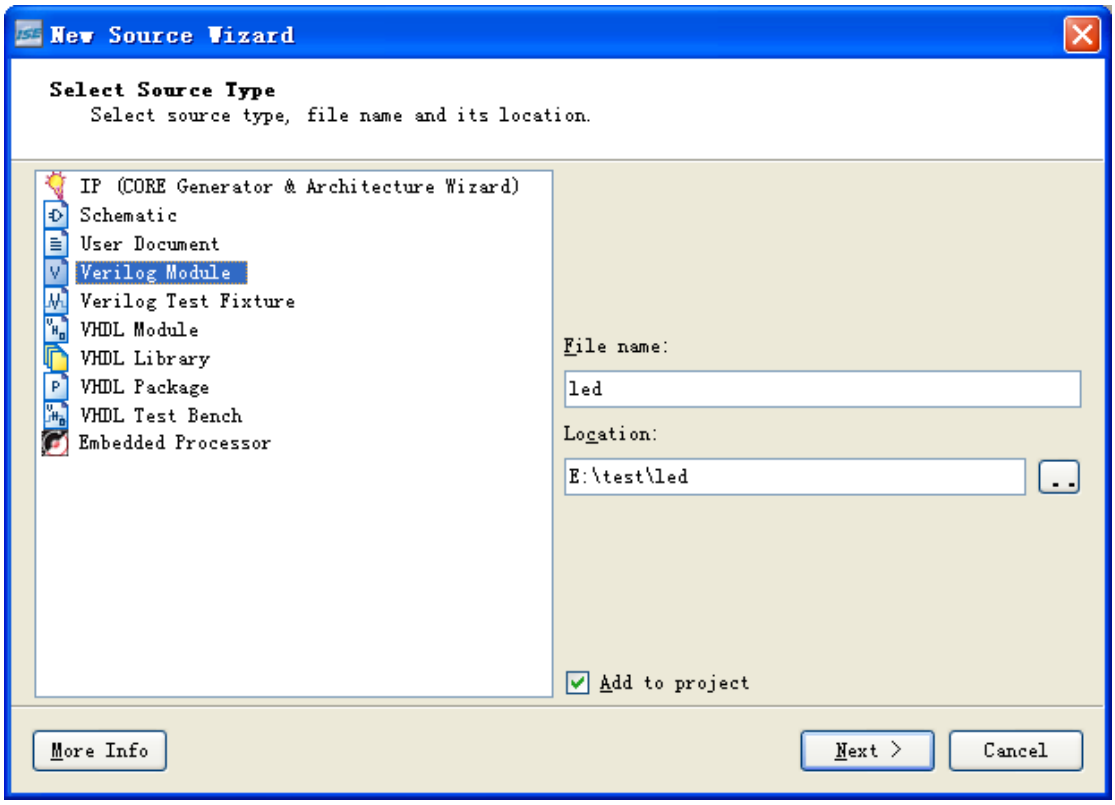
You need to add source files after set up project. Steps are as following:
Set up source file: click New source in design.



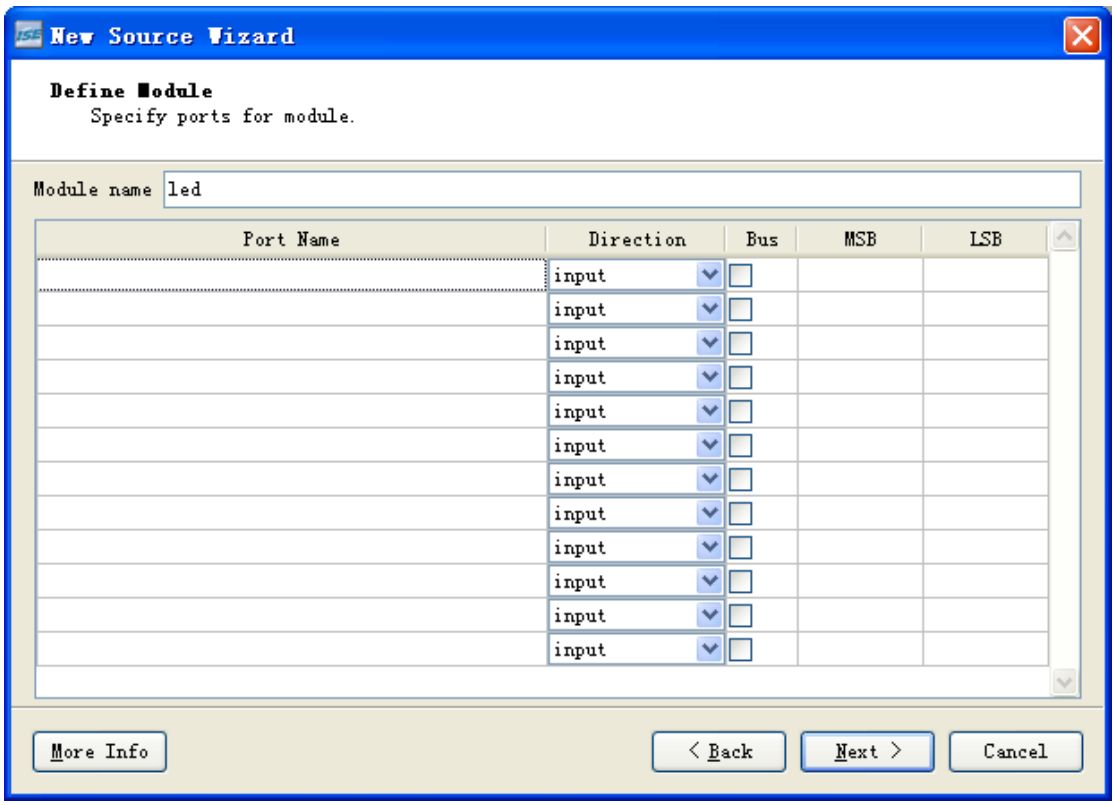
Or you may click right key of mouse on the icon xc3s1000-4ft256 in the dialog Module View to choose option New Source…



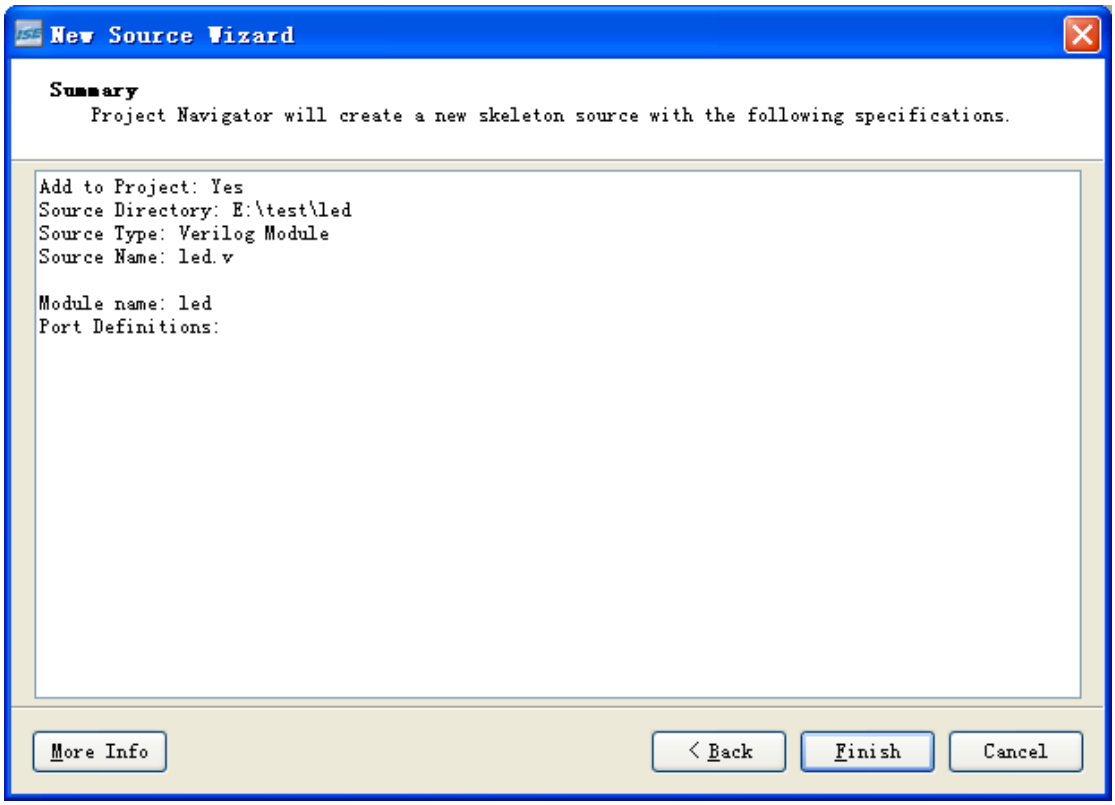
After choose New Source, the following dialog will pop out:



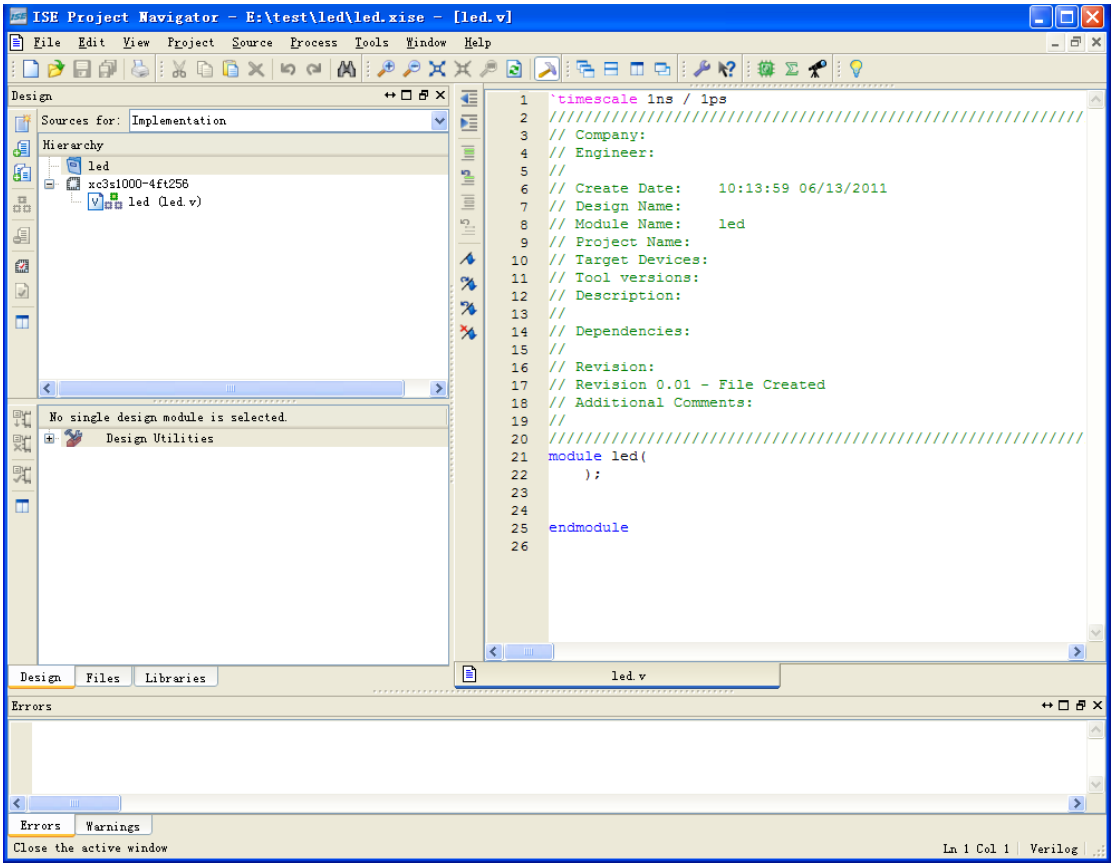
Fill the name of the source file to be generated in the column File Name on the right. The path normally is in the project folder which needn't to be changed without any special requirements. You have to choose Add to project. Than choose the source file type in the left icons. Click Next:



You can fill the source files' module names and pin definitions in the upper dialog. Or you don't input here. Input when write programs by yourself. Click Next:



Confirm the information, and then click finish. It will generate source file named led.v.



Input the program：

```
module sw_led(clk, rst, sw0, sw1, sw2, sw3, led0, led1, led2, led3, led4,
                    led5, led6, led7);
    input           clk;
    input           rst;
    input           sw0;
    input           sw1;
    input           sw2;
    input           sw3;
    output          led0;
    output          led1;
    output          led2;
    output          led3;
    output          led4;
    output          led5;
    output          led6;
    output          led7;

    wire            led0;
    wire            led1;
    wire            led2;
    wire            led3;
    wire            led4;
```

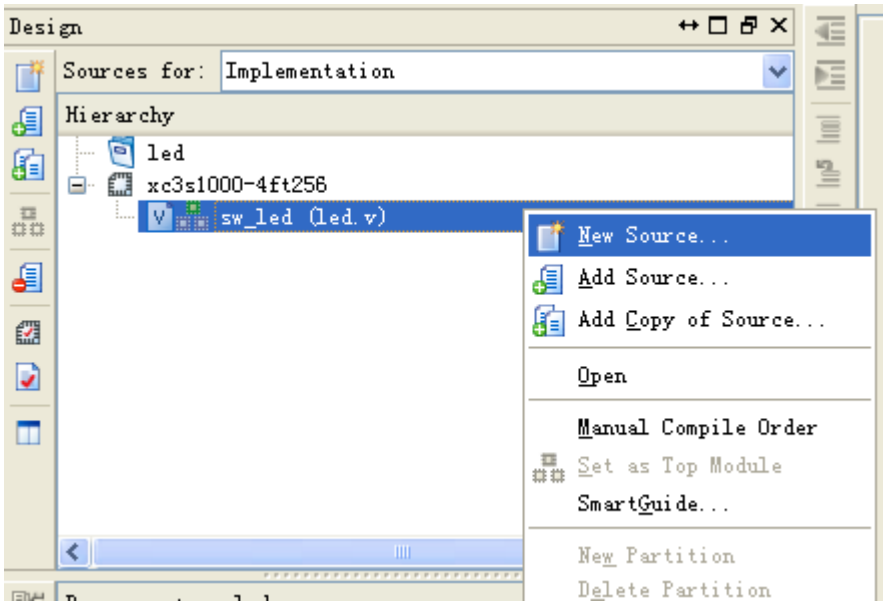
```
    wire                led5;
    wire                led6;
    wire                led7;

    wire    [3 :0] sw;
    reg     [7 :0] led;

    assign    sw ={sw0,sw1,sw2,sw3};
    assign    {led0,led1,led2,led3,led4,led5,led6,led7}=led;

    always @ ( posedge clk or negedge rst)
      begin
        if(!rst)
            led<='b0;
        else
            case ( sw )
            4'b0001:   led <= 8'b0000_0001;
            4'b0010:   led <= 8'b0000_0010;
            4'b0100:   led <= 8'b0000_0100;
            4'b1000:   led <= 8'b0000_1000;
            4'b0011:   led <= 8'b0001_0000;
            4'b0110:   led <= 8'b0010_0000;
            4'b1100:   led <= 8'b0100_0000;
            4'b1001:   led <= 8'b1000_0000;
            default:   led <= 8'b0000_0000;
            endcase
      end
endmodule
```

After input the program, you have to save the source file.

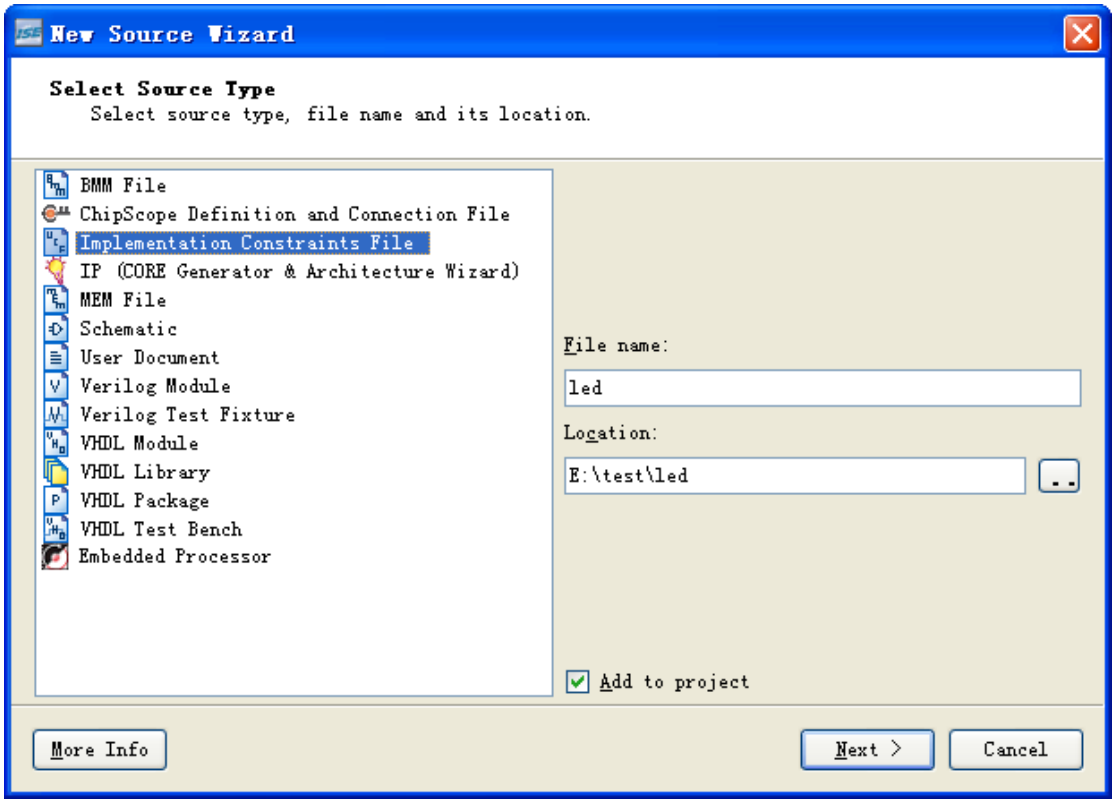
IV. Edit constraint

After input the source program, you can edit constraint and plan the direction of the placement and routing.

Click right in the source file and choose New Source

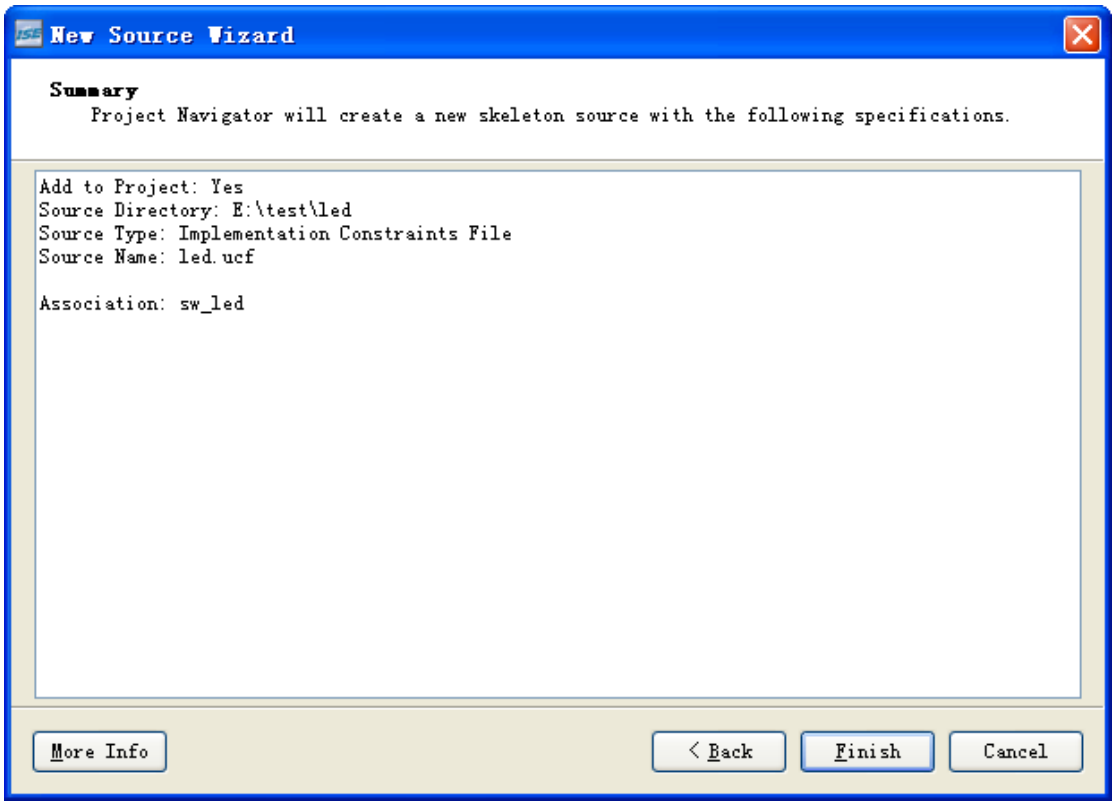


After choose New Source will come out the following dialog:



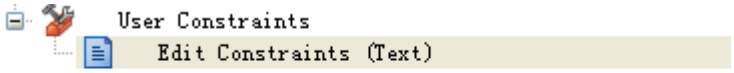
Fill the name of the constraint file to be generated in t he column File Name on the right. The path normally is in the project folder which needn't

to be changed without any special requirements. You have to choose Add to project，and then choose the constraint file type in the left icons. Click Next:



Confirm information and click Finish

Double click Edit Constraints (Text), and input program



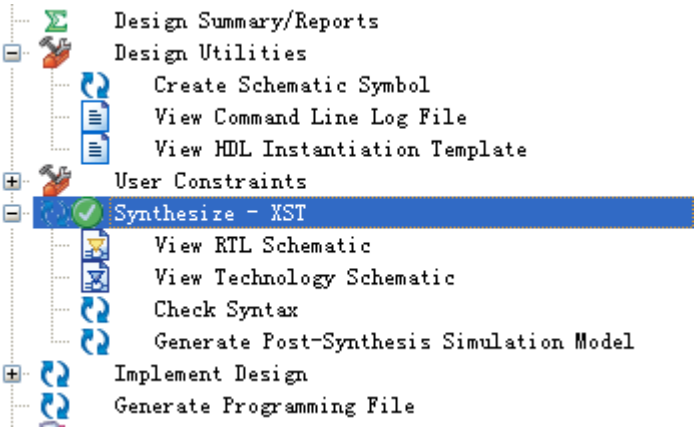

```
NET "clk"    LOC = "T9"    ;
NET "led0"    LOC = "A5"    ;
NET "led1"    LOC = "A7"    ;
NET "led2"    LOC = "A3"    ;
NET "led3"    LOC = "D5"    ;
NET "led4"    LOC = "B4"    ;
NET "led5"    LOC = "A4"    ;
NET "led6"    LOC = "C5"    ;
NET "led7"    LOC = "B5"    ;
NET "rst"    LOC = "K14"    ;
NET "sw0"    LOC = "R12"    ;
NET "sw1"    LOC = "P11"    ;
NET "sw2"    LOC = "R11"    ;
NET "sw3"    LOC = "M10"    ;
```

Save files

V. Synthesis

（一）Synthesis

In the dialog Process View, double click Synthesize - XST



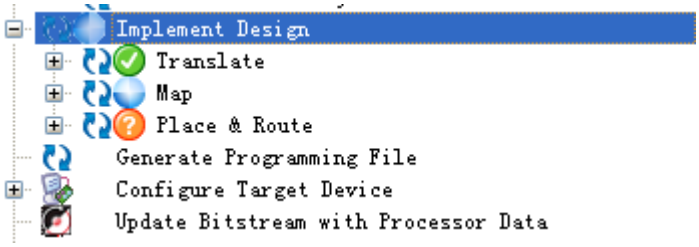
Here ISE will analysis the project module designed just now automatically. Check whether has grammar mistake or not（Check Syntax）. Check whether can synthesize module.

In the running window, double click Implement Design。ISE will run the following steps automatically:

Translate（Translate）： Translate the module description language to CLB language which can be mapped.

Map（Map）： Map the description language to the logic unit which can be existed in the FPGA.

Place and route（Place & Route）：Arrange and connect logic unit internal of the FPGA.

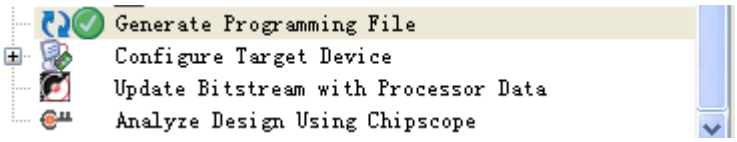


If succeed, we can check the FPGA source which have been used already in Design Summary.

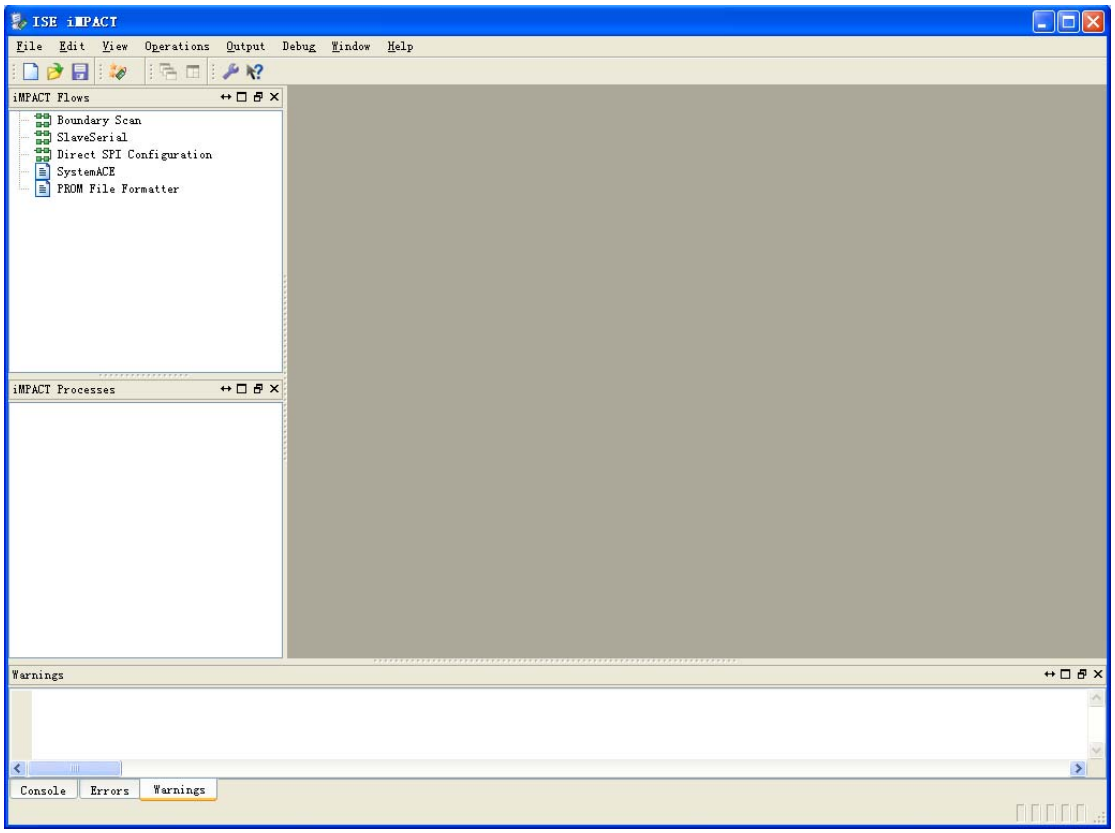
VI. Download（make sure development board has been connected to PC）

After placement and routing finished, you can download program to development board to debug. Connect the development board to PC correctly. The development board provides two download ways: JTAG and PROM. The difference is JTAG download used to online debugging which won't be saved if power off; PROM mode burns the program into

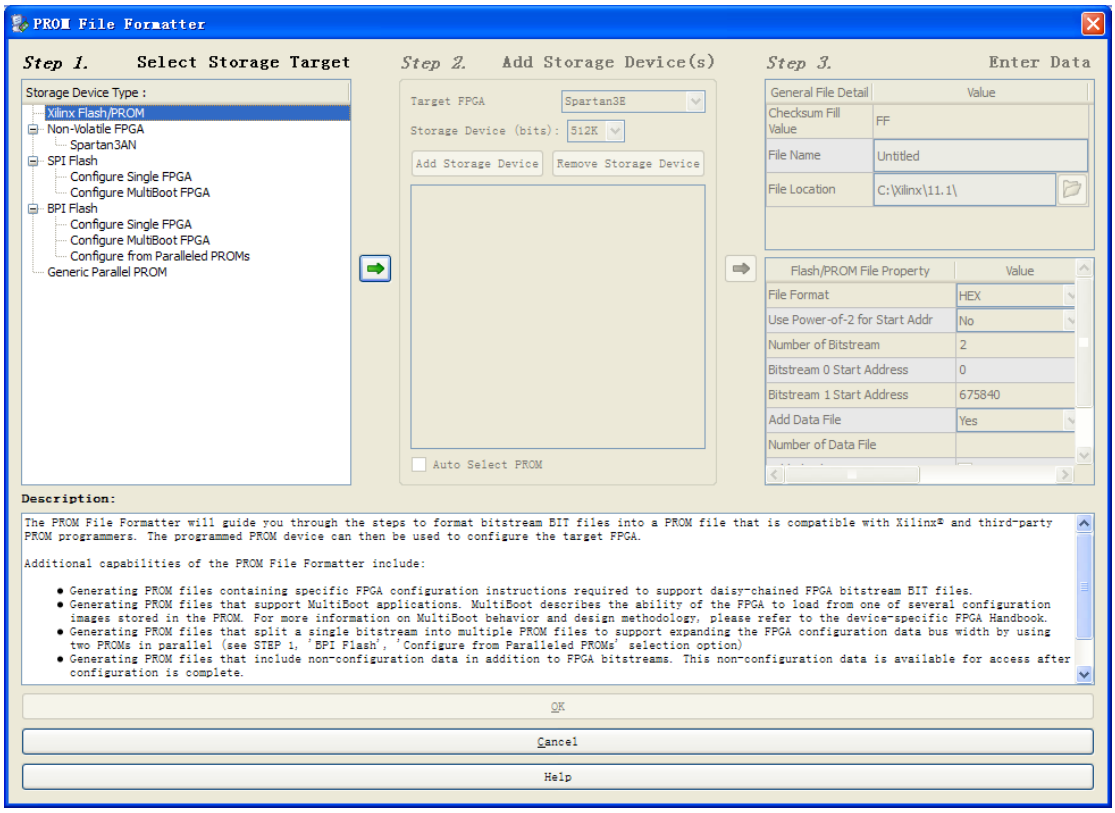
the memory which will load automatically when power on.
On Process View, double click icon Generate Programming File.



ISE will generate bit file for JTAG mode download. The green pair numbers on the left of Generate Programming File means the download files have been generated successfully.
Double click the icon Configure Device (iMPACT) in the dialog Process View and open the following dialog:

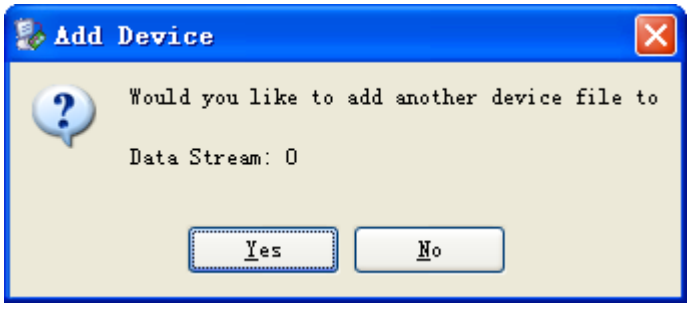


PROM mode download is save the program in the memory (the development board uses Xilinx company's xcf04s). When the development board is powered on, FPGA will load the programs in the memory automatically. Detailed operation steps are as following: double click PROM File Formatter，and comes out the dialog as the picture shows:



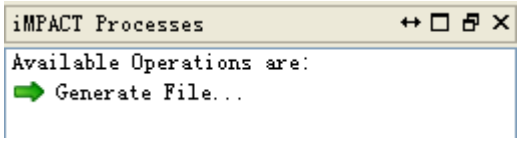
Click  ，choose xcf04s，click Add Storage Debice，click  ，fill the name of the file to be save in File Name，choose the save path in File Location. Click OK, pop the dialog:

Click OK，add file sw_led.bit, and pop the dialog:



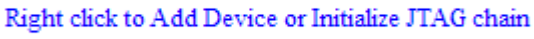
The upper dialog asks whether add another device file or not. Choose No:

Click OK. Set up PROM download file. Double click Generate File in iMPACT Processes:

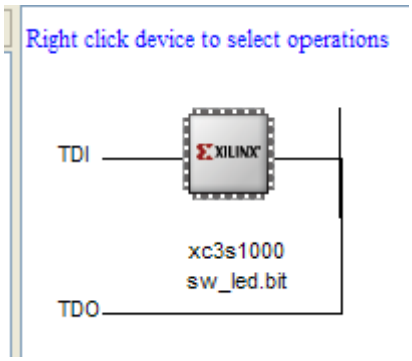


ISE will generate the hex PROM download file whose suffix is .MCS for us automatically. If succeed, the following picture will come out:

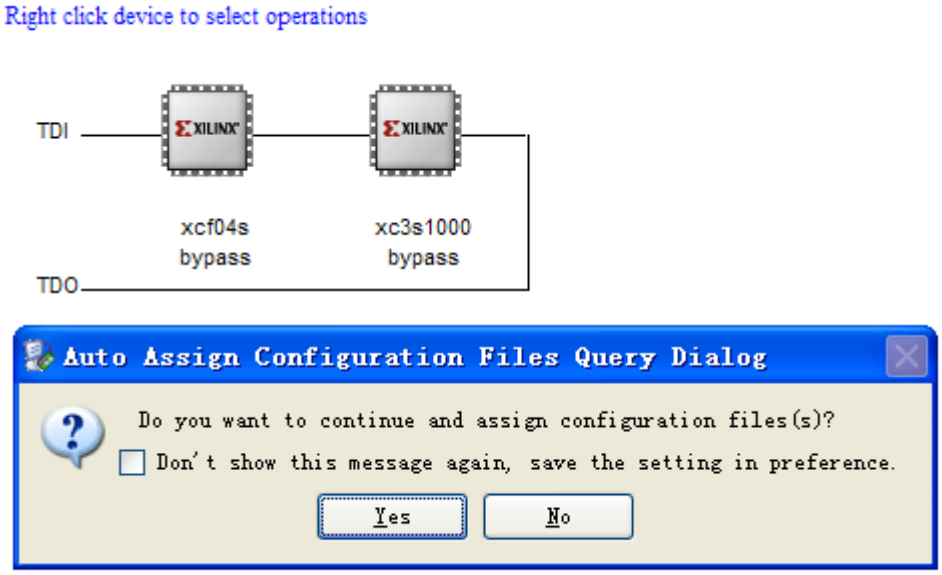
Double click Boundary Scan，and comes following dialog:



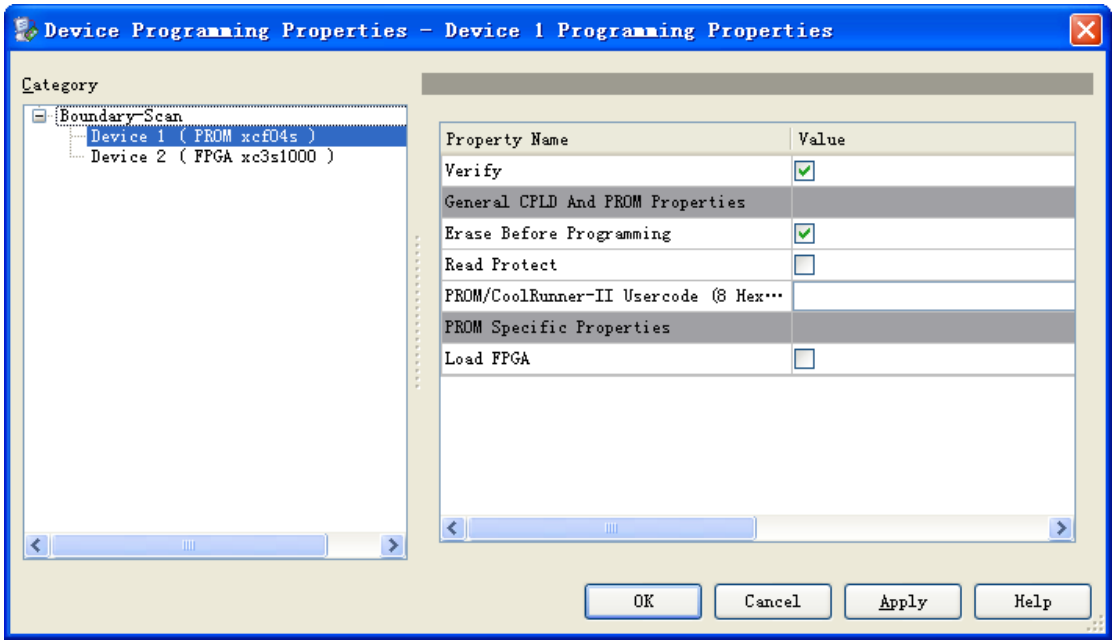
Click right，Add Xinlix Device，choose file sw_led.bit，and comes following dialog. Choose ok and see the link which scanned by ISE to development board:



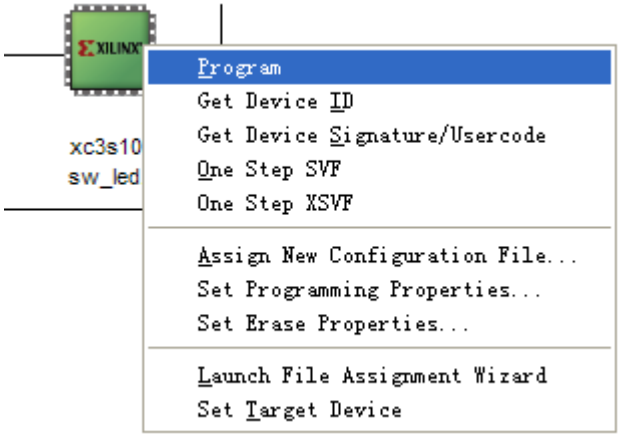
Add PROM，click  on the tool bar，comes dialog:



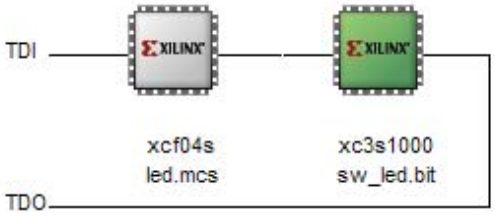
Choose Yes. Add generated file led.mcs in xcf04s. Add sw_led.bit into x3cs1000. Choose OK in the generated dialog.



Right click device icon and choose Program，



Then, can finish download. After download successfully, comes the following picture:



Finish all operation steps and can start to debug hardware on the development board.